Exhibit 25

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

ALPHA & OMEGA SEMICONDUCTOR, LTD., a Bermuda corporation; and ALPHA & OMEGA SEMICONDUCTOR, INC., a California corporation,

Plaintiffs and Counterdefendants,

v.

FAIRCHILD SEMICONDUCTOR CORP., a Delaware corporation,

Defendant and Counterclaimant.

AND RELATED COUNTERCLAIMS.

Case No. C 07-2638 JSW
(Consolidated with Case No. C-07-2664 JSW)

AOS'S SUPPLEMENTAL PRELIMINARY INVALIDITY CONTENTIONS FOR U.S. PATENT NOS. 6,429,481, 6,521,497, 6,710,406, 6,828,195, 7,148,111, AND 6,818,947 PURSUANT TO PATENT L.R. 3-3

Plaintiffs and Counterdefendants Alpha & Omega Semiconductor, Ltd. and Alpha & Omega Semiconductor, Inc. (collectively, "AOS") hereby provide the following supplemental invalidity claim charts for six asserted U.S. Patents, including U.S. Patent Nos. 6,429,481 ("the '481 Patent"), 6,521,497 ("the '497 Patent"), 6,710,406 ("the '406 Patent"), 6,828,195 ("the '195 Patent"), and 7,148,111 ("the '111 Patent"), which are collectively referred to as "the Mo Patents," and U.S. Patent No. 6,818,947 ("the '947 Patent"), pursuant to Patent L.R. 3-3 and the stipulated schedule in response to the two Disclosures of Asserted Claims and Preliminary Infringement Contentions prepared by Fairchild Semiconductor Corporation ("Fairchild").

For each asserted claim of the six asserted Fairchild Patents, AOS hereby: (1) identifies each prior art reference that either anticipates the claim or renders the claim obvious; (2) identifies where within each prior art reference each claim element is found; and (3) identifies whether these prior art references anticipate the claim or render the claim obvious and identifies combinations of prior art references that render the claim obvious.

As an initial matter, AOS notes that AOS is providing these invalidity claim charts while discovery from Defendant and Counterclaimant Fairchild is still ongoing. In particular, Fairchild has not provided complete discovery in response to AOS's interrogatories and requests for production relating to the six asserted Fairchild Patents. Depositions of persons involved in the drafting and prosecution of the asserted Fairchild parents will likely reveal more information that affects the conclusions herein. In addition, the Court has not yet construed the claims. Fairchild has not yet disclosed its theories of infringement; in particular, Fairchild has not yet disclosed its theories regarding certain recited properties of the claim elements. Accordingly, AOS reserves the right to supplement this response chart as it obtains further discovery from Fairchild or as otherwise permitted by the Court or the applicable rules.

I. Patent Local Rule 3-3 Response Chart

A. Identification of Prior Art

Presently, AOS intends to at least rely upon the following prior at patents and references:

- U.S. Patent No. 4,374,455
- U.S. Patent No. 5,072,266

- U.S. Patent No. 5,233,215
- U.S. Patent No. 5,268,586
- U.S. Patent No. 5,316,959
- U.S. Patent No. 5,349,224
- U.S. Patent No. 5,352,915
- U.S. Patent No. 5,405,794
- U.S. Patent No. 5,430,324
- U.S. Patent No. 5,460,985
- U.S. Patent No. 5,527,720
- U.S. Patent No. 5,597,765
- U.S. Patent No. 5,629,543
- U.S. Patent No. 5,674,766
- U.S. Patent No. 5,689,128
- U.S. Patent No. 5,701,023
- U.S. Patent No. 5,814,858
- U.S. Patent No. 5,864,159
- U.S. Patent No. 5,877,528
- U.S. Patent No. 5,910,669
- U.S. Patent No. 5,930,630
- U.S. Patent No. 5,998,833
- U.S. Patent No. 5,998,836
- U.S. Patent No. 6,031,265
- U.S. Patent No. 6,118,150
- U.S. Patent No. 6,404,025
- U.S. Patent No. 6,838,722
- European Patent Application No. 0159663
- Japanese Patent Application No. 1995066395
- Japanese Patent Application No. 1998214968

- Sze, S. M., "Physics of Semiconductor Devices," 2nd Ed., Bell Laboratories, 1981 ("the Sze book")
- Baliga, B. Jayant, "Power Semiconductor Devices," PWS Publishing Company, 1996 ("the Baliga book")
- Grant, D.A., Gowar, J., "Power MOSFETs: Theory and Applications," A. Wiley-Interscience Publication, 1989 ("the Grant book")

Additionally, AOS intends to rely on the inventor admissions made in the six asserted Fairchild Patents relating to the scope of prior art teaching, including but not limited to: U.S. Patent No. 6,429,481 and its Prosecution History; U.S. Patent No. 6,521,497 and its Prosecution History; U.S. Patent No. 6,710,406 and its Prosecution History; U.S. Patent No. 6,828,195 and its Prosecution History; U.S. Patent No. 7,148,111 and its Prosecution History; U.S. Patent No. 6,818,947 and its Prosecution History; as well as any patent applications filed in any other jurisdictions (including PCT applications) that are related to any of the six asserted Fairchild patents and their respective prosecution histories. AOS also reserves the right to rely upon other prior art uncovered during the course of discovery including, for example, Fairchild's own sales, offers for sale, use, or disclosures prior to the invention dates of the asserted Fairchild Patents.

B. Identification of Asserted Claim Elements of the Six Asserted Fairchild Patents in Prior Art

Presented below are locations within each listed prior art reference of the various elements of the asserted claims of the six asserted Fairchild Patents. Although specific references are made, each particular reference may contain additional discussion of a given claim element at other locations. Thus, the following description is made in an effort to identify each claim element as being contained in the respective references and is not intended to be an exhaustive listing of all teachings of a particular claim element within each prior art reference. AOS reserves the right to contend that other claims of the asserted Fairchild Patents are invalid; for example, if Fairchild amends its infringement contentions to assert other claims, AOS reserves the right to assert invalidity of those claims.

combinations of prior art that render the six asserted Fairchild Patents obvious in connection with further discovery, claim construction, the parties' exchange of expert reports, and as appropriate under Patent L.R. 3-6.

D. Additional Invalidity Claims against the Six Asserted Fairchild Patents

Besides the invalidity claims listed above under 35 U.S.C. §§102 and 103, AOS hereby asserts the following invalidity defenses against the six asserted Fairchild Patents under 35 U.S.C. §112. AOS reserves the right to revise and/or amend the following defenses pursuant to Federal Rule of Civil Procedure 26(e) and the Orders of record in this matter to the extent appropriate in light of further investigation and discovery regarding the defenses, the Court's construction of the claims at issue, and the review and analysis of expert testimony.

1. The '481 Patent

a. All asserted claims of the '481 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the term "abrupt junction;"

b. All asserted claims of the '481 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the term "abrupt junction;"

c. All asserted claims of the '481 Patent are invalid under 35 U.S.C. §112, ¶2 because the term "abrupt junction" renders the claims indefinite;

d. Claims 1-5 and 18-20 of the '481 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the phrase "the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor;"

e. Claims 1-5 and 18-20 of the '481 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement

with respect to the phrase "the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor;"

f. Claims 1-5 and 18-20 of the '481 Patent are invalid under 35 U.S.C. §112, ¶2 because the phrase "the depth of the junction, relative to the depth of the well, is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor" renders the claims indefinite;

g. Claims 6-14 and 21 of the '481 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the phrase "a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor;"

h. Claims 6-14 and 21 of the '481 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the phrase "a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor;"

i. Claims 6-14 and 21 of the '481 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the phrase "a depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor" renders the claims indefinite;

j. Claims 15-17 and 22 of the '481 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the phrase "a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor;"

k. Claims 15-17 and 22 of the '481 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the phrase "a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor;"

l. Claims 15-17 and 22 of the '481 Patent are invalid under 35 U.S.C. §112, ¶2 because the phrase "a depth of the heavy body junction relative to a maximum depth of the well, is adjusted so that a peak electric field in the substrate is spaced away from the trench when voltage is applied to the transistor" renders the claims indefinite;

m. Claim 22 of the '481 Patent is invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the phrase "the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate;"

n. Claim 22 of the '481 Patent is invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the phrase "the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate;" and

o. Claim 22 of the '481 Patent is invalid under 35 U.S.C. §112, ¶2 because the phrase "the second depth relative to a depth of the well is adjusted to eliminate the need for any layers disposed between the epitaxial layer and the substrate" renders the claims indefinite.

2. The '406 Patent

a. All asserted claims of the '406 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the term "abrupt junction;"

b. All asserted claims of the '406 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the term "abrupt junction;"

c. All asserted claims of the '406 Patent are invalid under 35 U.S.C. §112, ¶2 because the term "abrupt junction" renders the claims indefinite;

d. Claims 1-12 of the '406 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the phrase "a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor;"

e. Claims 1-12 of the '406 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the phrase "a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown initiation point is spaced away from the trench in the semiconductor;"

f. Claims 1-12 of the '406 Patent are invalid under 35 U.S.C. §112, ¶2 because the phrase "a location of the abrupt junction relative to the depth of the well is adjusted so that a transistor breakdown

initiation point is spaced away from the trench in the semiconductor" renders the claims indefinite;

g. Claims 13-32 of the '406 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the phrase "the depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor;"

h. Claims 13-32 of the '406 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the phrase "the depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor;" and

i. Claims 13-32 of the '406 Patent are invalid under 35 U.S.C. §112, ¶2 because the phrase "the depth of the heavy body relative to a depth of the well is adjusted so that breakdown of the transistor originates in the semiconductor in a region spaced away from the trenches when voltage is applied to the transistor" renders the claims indefinite.

3. The '195 Patent

a. All asserted claims of the '195 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the term "abrupt junction;"

b. All asserted claims of the '195 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the term "abrupt junction;"

c. All asserted claims of the '195 Patent are invalid under 35 U.S.C. §112, ¶2 because the term "abrupt junction" renders the claims indefinite.

4. The '111 Patent

a. Claims 29-35 of the '111 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the phrase "adjusting a dopant profile of the plurality of heavy body regions;"

b. Claims 29-35 of the '111 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the phrase "adjusting a dopant profile of the plurality of heavy body regions;"

c. Claims 29-35 of the '111 Patent are invalid under 35 U.S.C. §112, ¶2 because the phrase "adjusting a dopant profile of the plurality of heavy body regions" renders the claims indefinite;

d. Claims 29-35 of the '111 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the written description requirement with respect to the phrase "resulting in avalanche current that is substantially uniformly distributed;"

e. Claims 29-35 of the '111 Patent are invalid under 35 U.S.C. §112, ¶1 for failing to meet the enablement requirement with respect to the phrase "resulting in avalanche current that is substantially uniformly distributed;" and

f. Claims 29-35 of the '111 Patent are invalid under 35 U.S.C. §112, ¶2 because the phrase "adjusting a dopant profile of the plurality of heavy body regions" renders the claims indefinite.

5. The '947 Patent

a. All claims of the '947 Patent are invalid under 35 U.S.C. §112, ¶1 because FIGS. 4A-4B and their associated text are new matter that were introduced into the specification after the initial filing of the application.

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AOS has not yet completed its investigation of this matter and reserves the right to identify additional grounds that invalidate the six asserted Fairchild Patents obvious in connection with further discovery, claim construction, the parties' exchange of expert reports, and as appropriate under Patent L.R. 3-6.

Dated: March 3, 2008

MORGAN, LEWIS & BOCKIUS LLP

By: _____
Andrew J. Wu
Attorneys for Plaintiffs and Counterdefendants
ALPHA & OMEGA SEMICONDUCTOR, LTD. AND ALPHA & OMEGA SEMICONDUCTOR, INC.

CERTIFICATE OF SERVICE

I am employed in the City of Palo Alto, County of Santa Clara, State of California, I am over the age of 18 years and not a party to the within action. My business address is 2 Palo Alto Square, 3000 El Camino Real, Palo Alto, California 94306. On March 3, 2008, I caused copies of the attached document(s) described as follows:

AOS'S SUPPLEMENTAL PRELIMINARY INVALIDITY CONTENTIONS FOR U.S. PATENT NOS. 6,429,481, 6,521,497, 6,710,406, 6,828,195, 7,148,111, AND 6,818,947 PURSUANT TO PATENT L.R. 3-3;

to be served on:

Eric P. Jacobs, Esq.
Igor Shoiket, Esq.
Matthew Hulse, Esq.
Leonard J. Augustine, Esq.
Priya Sreenivasan, Esq.
TOWNSEND & TOWNSEND
2 Embarcadero Center, 8th Floor
San Francisco, CA 94111

☐ (BY OVERNIGHT DELIVERY) I caused each such envelope to the addressee(s) noted above, with charges fully prepaid, to be sent by overnight delivery from Palo Alto, California. I am readily familiar with the practice of Morgan, Lewis & Bockius LLP for collection and processing of correspondence for overnight delivery, said practice being that in the ordinary course of business, mail is placed with the overnight delivery service on the same day as it is placed for collection.

☐ (BY FIRST CLASS MAIL) I caused each such envelope to the addressee(s) noted above, with postage thereon fully prepaid, to be placed in the United States mail in Palo Alto, California. I am readily familiar with the practice of Morgan, Lewis & Bockius LLP for collection and processing of correspondence for mailing, said practice being that in the ordinary course of business mail is deposited in the United States Postal Service the same date as it is placed for collection.

☐ (BY PERSONAL SERVICE) The person whose name is noted below caused to be delivered by hand each such envelope to the addressee(s) noted above.

☐ (BY FACSIMILE) The person whose name is noted below caused to be transmitted by facsimile each such document to the addressee(s) noted above.

☒ (BY ELECTRONIC MAIL) The person whose name is noted below caused to be transmitted by electronic mail each such document to the addressee(s) noted above.

I declare under penalty of perjury under the laws of the State of California that the foregoing is true and correct. Executed at Palo Alto, California, on March 3, 2008.

Yalei Sun